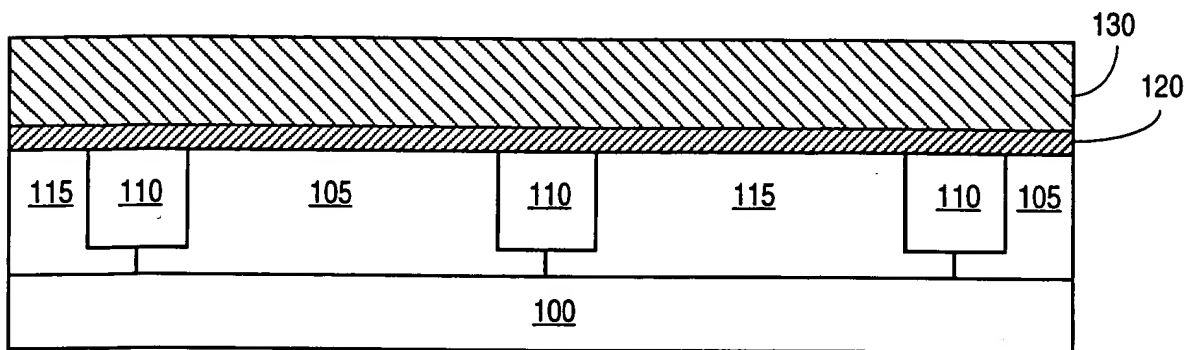
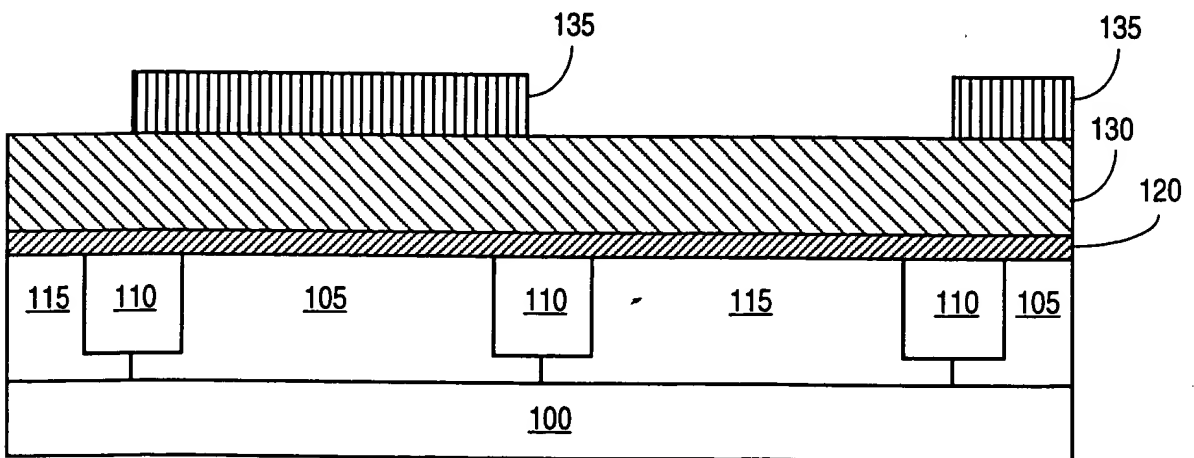


**Fig. 1**

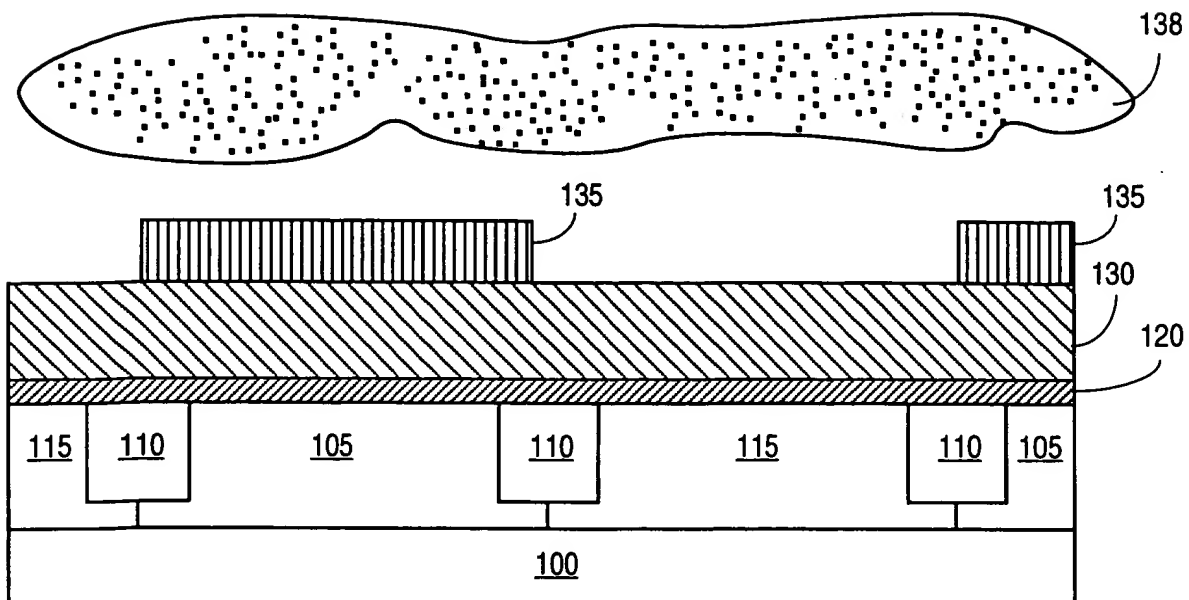


**Fig. 2**

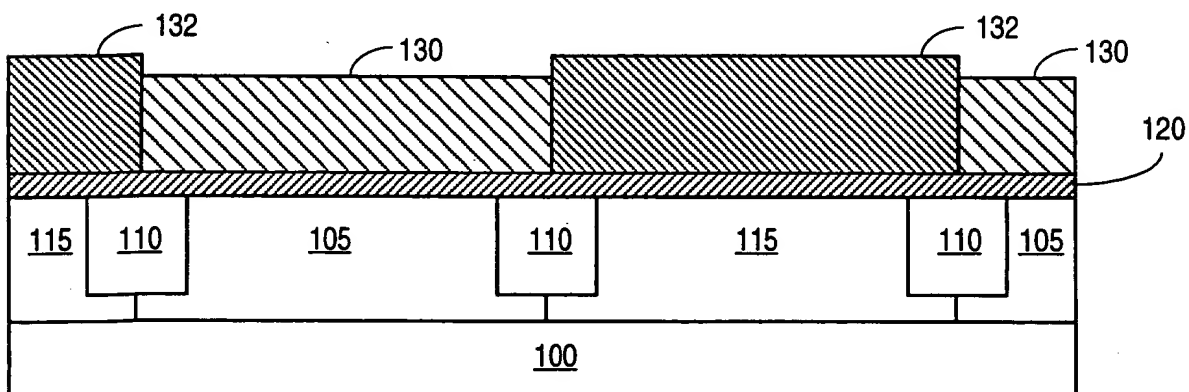


**Fig. 3**

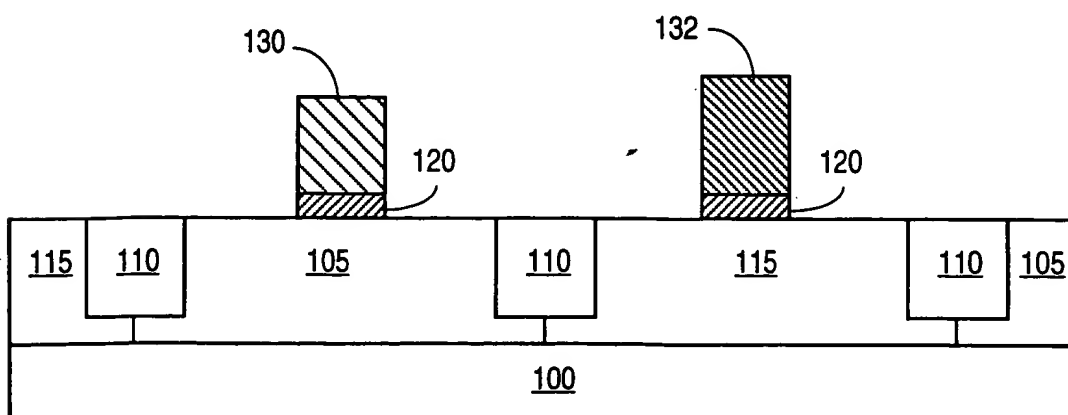
0951705-030200



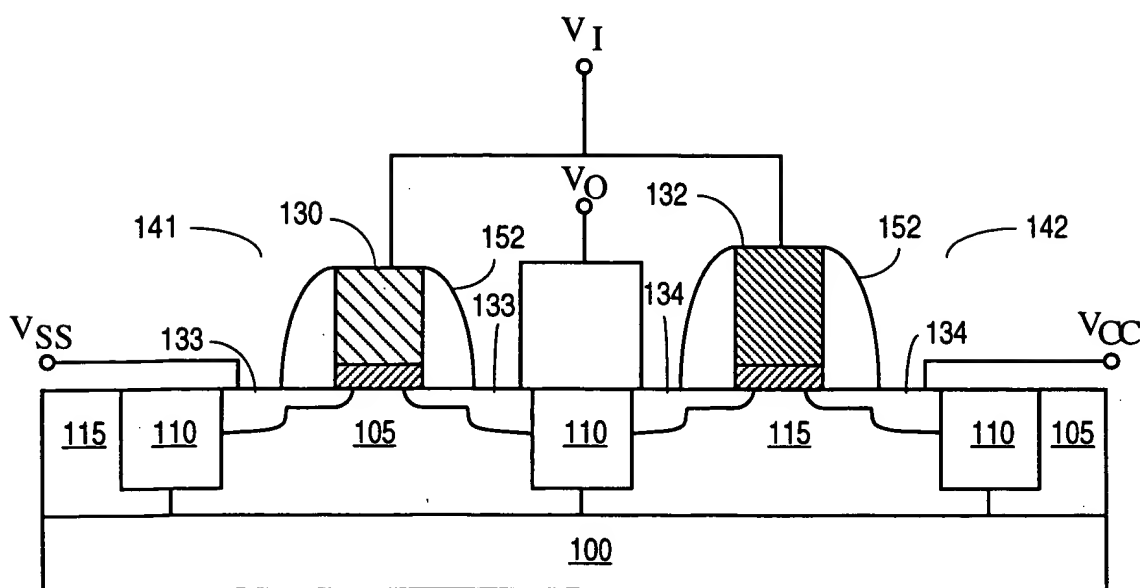
**Fig. 4**

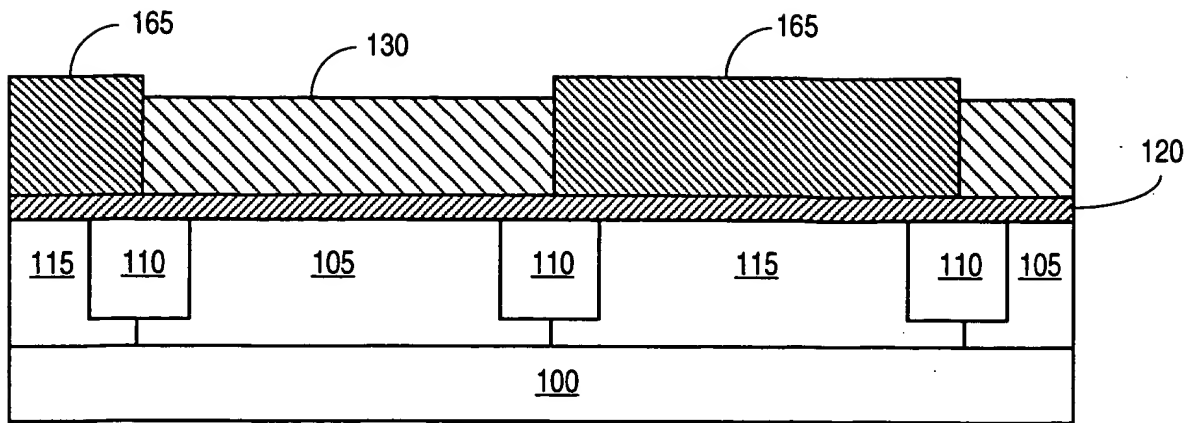


**Fig. 5**

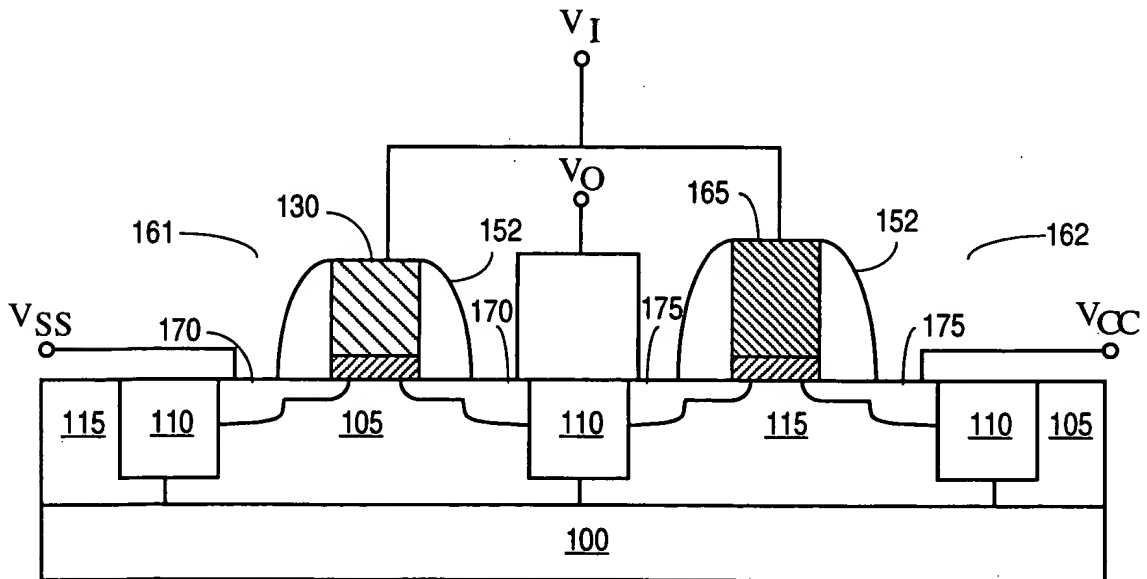


**Fig. 6**

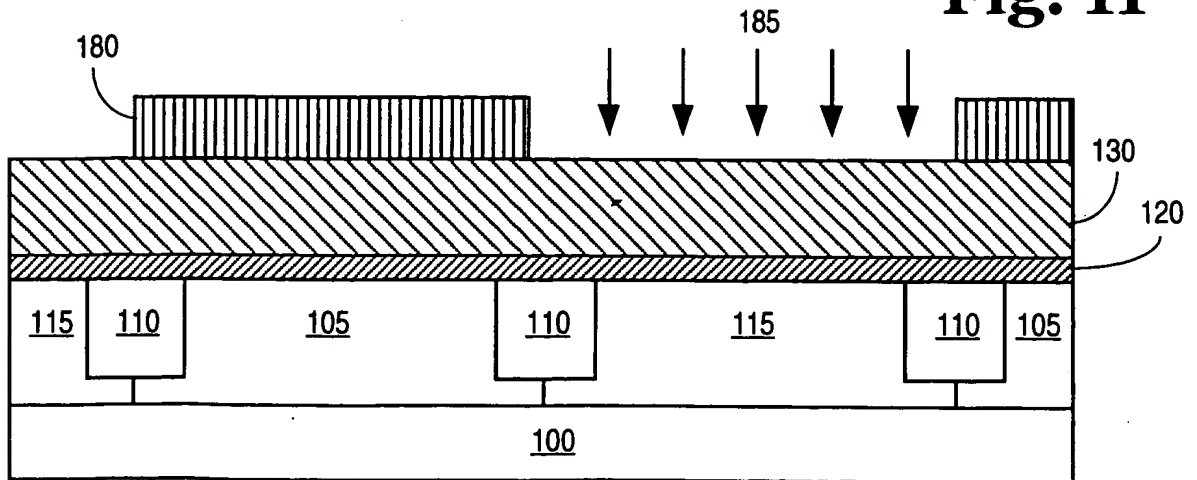




**Fig. 10**



**Fig. 11**



**Fig. 12**

FIG. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 100. A gate stack is formed on the substrate 100, comprising a gate dielectric 130 and a gate electrode 190. The gate stack is divided into three regions: a first region 115, a second region 110, and a third region 115. A dielectric layer 120 is formed on top of the gate stack. The dielectric layer 120 is divided into three regions: a first region 130, a second region 190, and a third region 120.

**Fig. 14**